



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent Application of)

SHIMAMOTO *et al.*)

Application Number: 10/020,314)

Filed: December 18, 2001)

For: FABRICATING METHOD OF SEMICONDUCTOR)
INTEGRATED CIRCUITS)

ATTORNEY DOCKET NO. HITA.0143)

Art unit: 2823

Examiner:

NGUYEN, KHIEM D.

#8/ Election
3/31/03
VS

Honorable Assistant Commissioner
for Patents
Washington, D.C. 20231

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TECHNOLOGY CENTER 2800

RESPONSE AND AMENDMENT UNDER 37 C.F.R. §1.111

Sir:

This is in response to the Office Action dated February 26, 2003, the shortened period for response to which is set to expire on March 26, 2003. Applicants hereby provisionally elect the continuing prosecution of Species I, drawn to a fabricating method of a semiconductor integrated circuit comprising forming a ruthenium electrode of a capacitor with high-k material on a semiconductor substrate by a chemical vapor deposition method in a sub-atmospheric pressure using an organoruthenium compound as a precursor, with traverse. Claims 1 through 12 and 16 through 19 pertain to the elected species, wherein claim 12 is believed generic to all of the identified species.